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S1	376	(712/200).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:45
S2	251	(712/219).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:45
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S4	7	(replay\$3 or reissu\$3 or re?execut\$3 or (execut\$3 adj1 again) or re?process\$3) with ((track\$3 or count\$3 or follow\$3) near4 (tim\$3 near4 period\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:48
S5	53	(replay\$3 or reissu\$3 or re?execut\$3 or (execut\$3 adj1 again) or re?process\$3) same ((track\$3 or count\$3 or follow\$3) near4 (tim\$3 near4 period\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:52
S6	130	(replay\$3 or reissu\$3 or re?execut\$3 or (execut\$3 adj1 again) or re?process\$3) same ((track\$3 or count\$3 or follow\$3) with (tim\$3 near4 period\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:52
S7	3	(replay\$3 or reissu\$3 or re?execut\$3 or (execut\$3 adj1 again) or re?process\$3) same ((track\$3 or count\$3 or follow\$3) with (tim\$3 near4 period\$1 near4 (increas\$3 or add\$3)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:54
S8	3	(replay\$3 or reissu\$3 or re?execut\$3 or (execut\$3 adj1 again) or re?process\$3) same ((track\$3 or count\$3 or follow\$3) same (tim\$3 near4 period\$1 near4 (increas\$3 or add\$3)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:55
S9	1	(replay\$3 or reissu\$3 or re?execut\$3 or (execut\$3 adj1 again) or re?process\$3) same ((track\$3 or count\$3 or follow\$3) same (tim\$3 near4 period\$1 near4 (elongat\$3)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 09:55

S10	20	"replay".ti. and ("712").clas.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/02/08 10:53
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1 On load latency in low-power caches

Kim, S.; Vijaykrishnan, N.; Irwin, M.J.; John, L.K.;

Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on , 25-27 Aug. 2003

Pages:258 - 261

[\[Abstract\]](#) [\[PDF Full-Text \(526 KB\)\]](#) IEEE CNF

2 SSD: an affordable fault tolerant architecture for superscalar processors

Seongwoo Kim; Somani, A.K.;

Dependable Computing, 2001. Proceedings. 2001 Pacific Rim International Symposium on , 17-19 Dec. 2001

Pages:27 - 34

[\[Abstract\]](#) [\[PDF Full-Text \(768 KB\)\]](#) IEEE CNF

3 Memory Ordering: A Value-Based Approach

Cain, H.W.; Lipasti, M.H.;

Micro, IEEE , Volume: 24 , Issue: 6 , Nov.-Dec. 2004

Pages:110 - 117

[\[Abstract\]](#) [\[PDF Full-Text \(136 KB\)\]](#) IEEE JNL

4 Fault tolerance through re-execution in multiscalar architecture

Rashid, F.; Saluja, K.K.; Ramanathan, P.;

Dependable Systems and Networks, 2000. DSN 2000. Proceedings International Conference on , 25-28 June 2000

Pages:482 - 491

[\[Abstract\]](#) [\[PDF Full-Text \(3440 KB\)\]](#) IEEE CNF

5 Cyclone: a broadcast-free dynamic instruction scheduler with selective replay

Ernst, D.; Hamel, A.; Austin, T.;

Computer Architecture, 2003. Proceedings. 30th Annual International Symposium
on , 9-11 June 2003
Pages:253 - 262

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